CLAIMS

1. A power management controller for instantaneous frequency-based microprocessor power management, comprising:

   a first PLL that generates a first core source clock signal at a first frequency based on a bus clock signal;

   a second PLL that generates a second core source clock signal at a programmable frequency based on a frequency control signal and said bus clock signal;

   select logic that selects between said first and second core source clock signals to provide a core clock signal for the microprocessor based on a select signal; and

   source control logic that detects power conditions via at least one power sense signal, that provides said frequency control signal according to said power conditions, and that provides said select signal.

2. The power management controller of claim 1, wherein said second PLL generates a lock signal when said second core source clock signal is at a frequency indicated by said frequency control signal.

3. The power management controller of claim 2, wherein said source control logic controls said select signal to switch from said first core source clock signal to said second core source clock signal in response to said lock signal.

4. The power management controller of claim 3, wherein said source control logic controls said select logic to switch said core clock signal from said first core source clock signal to said second core source clock signal within one clock cycle of said bus clock signal.

5. The power management controller of claim 1, wherein said first frequency is associated with the full operating frequency of the microprocessor.

6. The power management controller of claim 5, wherein said second core source clock signal is programmed to a reduced frequency appropriate for reduced power conditions.

7. The power management controller of claim 1, wherein said at least one power signal is provided by any of a plurality of mechanisms including registers, transducers and power signals.

8. A microprocessor, comprising:

a sense interface receiving at least one power sense signal indicative of power conditions;

a clock source controller, coupled to said sense interface, that provides a select signal for switching between first and second core clock signals, that provides a core ratio bus indicative of a reduced core clock frequency, and that receives a lock signal indicating that said reduced core clock frequency is operative;

a primary PLL, coupled to said clock source controller, that provides said first core clock signal at a first frequency based on a bus clock signal;

a programmable PLL, coupled to said clock source controller, that generates said second core clock signal at a frequency based on said core ratio bus and said bus clock signal and that provides said lock signal; and

select logic that selects between said first and second core clock signals to provide a core clock signal based on said select signal.

9. The microprocessor of claim 8, wherein said sense interface receives at least one external power sense signal.

10. The microprocessor of claim 8, further comprising at least one internal programmable register coupled to said sense interface.

11. The microprocessor of claim 8, wherein said clock source controller determines a reduced power level sufficient to meet said power conditions, and provides said core ratio bus to indicate a core clock frequency to achieve said reduced power level.

12. The microprocessor of claim 11, wherein said clock source controller switches said select signal to select said programmable PLL in response to receiving said lock signal.

13. The microprocessor of claim 12, wherein said clock source controller switches said select signal to select said primary PLL in response to changes of said power conditions while said programmable PLL is selected.

14. A method of instantaneous processor power management, comprising:

generating a first source clock at a full power frequency based on a bus clock;

generating a second source clock at a reduced power frequency based on the bus clock and a frequency control input;

sensing power conditions; and

switching between the first and second source clock signals based on sensed power conditions.

15. The method of 14, wherein said sensing power conditions comprises monitoring at least one power sense signal.

16. The method of claim 15, further comprising programming a register to indicate a reduced power level, and wherein said monitoring at least one power sense signal comprises reading the register.

17. The method of claim 14, further comprising:

initially selecting the first source clock signal;

providing the frequency control input based on sensed power conditions to indicate the reduced power frequency;

ramping the second source clock signal to the reduced power frequency in response to the frequency control input;

providing a lock indication when the second source clock signal achieves the reduced power frequency; and

switching to the second source clock signal when the lock indication is provided.

18. The method of claim 17, wherein said switching to the second source clock signal comprises switching within one bus clock cycle.

19. The method of claim 17, wherein said sensing power conditions comprises sensing a different power condition after said switching to the second source clock signal, and wherein said switching between the first and second source clock signals comprises switching back to the first source clock signal.

20. The method of claim 19, wherein said switching back to the first source clock signal comprises switching within one bus clock cycle.